Modified PTO/SB/33 (10-05)

PRE-APPEAL BRIEF REQUEST FOR REVIEW	Docket Number Q78894	
Mail Stop AF Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450	Application Number 10/758,040	Filed January 16, 2004
	First Named Inventor Sung-kyu CHOI	
	Art Unit 2111	Examiner Christopher E. LEE

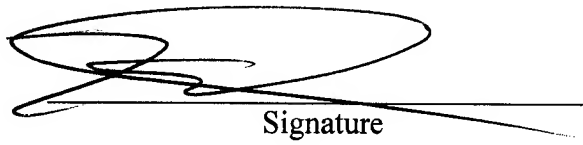
WASHINGTON OFFICE
23373
CUSTOMER NUMBER

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal

The review is requested for the reasons(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

☑ I am an attorney or agent of record.
Registration number 59,043



Signature

Mark E. Wallerson
Typed or printed name

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July 18, 2007
Date

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Sung-kyu CHOI

Docket No: Q78894

Appln. No.: 10/758,040

Group Art Unit: 2111

Confirmation No.: 6125

Examiner: Christopher E. LEE

Filed: January 16, 2004

For: APPARATUS AND METHOD FOR CONNECTING PROCESSOR TO BUS

PRE-APPEAL BRIEF REQUEST FOR REVIEW

MAIL STOP AF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to the Pre-Appeal Brief Conference Pilot Program, and further to the Examiner's Final Office Action dated January 18, 2007, Applicant files this Pre-Appeal Brief Request for Review. This Request is also accompanied by the filing of a Notice of Appeal. Applicant now turns to the rejections at issue.

Claim 1 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Bourke et al. (U.S. Patent No. 5,509,124, hereafter "Bourke") in view of Barrenscheen et al. (U.S. Patent Application Publication No. 2003/0084226, hereafter "Barrenscheen"). Claims 2-6 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Masayuki et al. (JP 2000-92365A, hereafter "Masayuki") in view of Barrenscheen. Claims 7-9 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Masayuki in view of Barrenscheen, and further in view of Sodos (U.S. Patent No. 5,239,651). Claim 10 is rejected under 35 U.S.C. § 103(a) as being

unpatentable over Masayuki in view of Barrenscheen and Luo et al. (U.S. Patent No. 6,265,885, hereafter "Luo").

Claim 1 recites in part:

> wherein the multiplexer receives first data from the processor and transfers the received first data to a first memory through a synchronous data bus synchronized with the processor, or receives second data from the first memory through the synchronous data bus and transfers the received second data to the processor.

The Examiner asserts that Barrenscheen discloses this feature of the claim and apparently reads the claimed multiplexer on Bus Interface (BI1) as disclosed by Barrenscheen.

Applicant respectfully submits that the Bus Interface BI1 is not a multiplexer. Instead, Bus Interfaces BI1-BI4 are used to connect the data transmission device DTU to the first through fourth buses BUS1-BUS4, respectively. Consequently, Bus Interface BI1 does not perform the functions of and is not described as a multiplexer in Barrenscheen.

The Examiner maintains that the claimed multiplexer reads on the Bus Interface (BI1), and asserts that:

> [T]he recited claiming language "multiplexer," and its function in the exemplary claim 1 are interpreted as the bus interface BI1 performs the functions of and is described as the claimed subject matter "multiplexer" in Barrenscheen.[3]

Applicant respectfully submits that claim 1 would not have been rendered obvious by Bourke and Barrenscheen. There is simply no disclosure in Barrenscheen that the Bus interface, BI1 acts as or performs the functions of a multiplexer.

[3] Page 17 of the Office Action dated January 18, 2007.

The Examiner also maintains that Barrenscheen discloses that BUS1 is synchronized with the processor, and cites paragraph [0035] of Barrenscheen as allegedly disclosing this feature of claim 1. However, paragraph [0035] merely discloses that when the data transmission device (DTU) is used as a DMA controller, it can transmit data between devices connected to the same bus or between devices connected between different buses autonomously. There is simply no disclosure in Barrenscheen that the BUS1 is synchronized with a processor.

With respect to independent claims 2, 4, and 10, the Examiner asserts that Masayuki teaches both a synchronous bus and an asynchronous bus as required by independent claims 2, 4, and 10, and cites bus 34 and bus 33 of Masayuki as allegedly respectively reading on the claimed synchronous and asynchronous buses.

Applicant respectfully submits that it appears that the Examiner is merely assuming that CPU bus 34 is (synchronous) synchronized with CPU 41, and that image data bus 33 is (asynchronous) not synchronized with CPU 41 because image data bus 33 is not directly connected to CPU 41 in Fig. 2. However, nowhere does Masayuki disclose that image data bus 33 is asynchronous. Moreover, Masayuki does not disclose any terms related to "synchronous" and "asynchronous".

The Examiner simply asserts that:

> Even though the Applicant argues that Masayuki does not disclose any terms related to 'synchronous' and 'asynchronous', Masayuki discloses CPU (i.e., processor) and CPU bus (i.e., synchronized bus with said CPU), and further, image data bus (i.e., asynchronous data bus) being synchronized by Sync

Generator in the Signal Processor, not being synchronized with said CPU (i.e., processor).[4]

Applicant respectfully submits that claim 2 and analogous claims 4 and 10 would not have been rendered obvious over Masayuki.

First, there is simply no teaching or suggestion in Masayuki of synchronous and asynchronous buses. Masayuki teaches a method of preventing delays on an image data bus and improving signal processing efficiency by controlling/managing the read-out and write-in process of storage means connected to the image data bus. Nowhere does Masayuki expressly disclose synchronizing a data bus with a processor.

At best, Masayuki discloses that the sink generator 26 may provide a synchronization signal (for example a clock signal), not to the image bus 33, but only to the timing generator 13, wherein the timing generator 13 generates a horizontal synchronization signal and a vertical synchronization signal controlling every circuit of the image generator (see the signal lines of FIG. 1 and paragraphs [0014] and [0017]). In other words, the synchronization signal generated by the sink generator 26 is only for generating a horizontal synchronization signal and a vertical synchronization signal controlling every circuit of the image generator 10.

Applicant also respectfully submits that it appears that the image bus 33 is synchronized with CPU 41 as CPU bus 34, because the image bus 33 is directly connected to the CPU bus 34, not via a buffer, as illustrated in FIG. 2 of Masayuki. Therefore, the Examiner's assertion that image bus 33 is an asynchronous data bus not synchronized with the processor and synchronized with the sink generator is clearly erroneous.

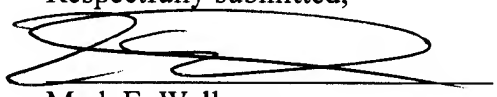
[4] Pages 18-19 of the Office Action dated January 18, 2007.

Further, the fact that Masayuki teaches a signal processing unit which prevents delay of image data does not necessarily mean that this "inherently" teaches that the image data bus is synchronized with the CPU as alleged by the Examiner.[5]

Second, the comments in the Office Action regarding inherency are not understood; the principle of inherency is applicable only with respect to 35 U.S.C. §102 rejections. Inherency and obviousness are distinct concepts. A retrospective view of inherency is not a substitute for some teaching or suggestion that supports the selection and use of the elements in the particular claimed combination. In deciding that a novel combination would have been obvious, there must be a supporting teaching in the prior art; for that which may be inherent is not necessarily known, and obviousness cannot be predicated on what is unknown. See In re Newell, 13 U.S.P.Q.2d 1248, 1250 (Fed. Cir. 1989).

Accordingly, Applicant respectfully submits that independent claims 1, 2, 4, and 10 as well as dependent claims 3, and 5-9 should be allowable because the cited references do not teach or suggest all of the features of the claims.

Respectfully submitted,



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[5] Page 19 of the Office Action dated January 18, 2007.